A PARALLEL SENSE AMPLIFIER WITH MIRRORING OF THE CURRENT TO BE MEASURED INTO EACH REFERENCE BRANCH

PRIORITY CLAIM

[1] This application claims priority from Italian patent application No. MI2003A 000075, filed January 20, 2003, which is incorporated herein by reference.

TECHNICAL FIELD

[2] The present invention relates generally to a parallel sense amplifier.

BACKGROUND

[3] Sense amplifiers are commonly used in several applications, such as for reading non-volatile memory devices. A sense amplifier consists of a circuit that can measure an input signal at low level (such as a current).

[4] A standard sense amplifier compares the input current with a reference value. For example, in a non-volatile memory device, the current provided by a selected memory cell is compared with the current provided by a reference cell. Typically, the sense amplifier includes a current mirror with unbalanced loads. A portion of the reference current provided to an input branch (generally one half of the reference current) is mirrored into an output branch connected to the memory cell. In this way, the voltage at a node of the output branch increases or decreases according to whether the current of the memory cell is lower or higher than one half of the reference current. A comparator compares this voltage with a voltage at a node of the input branch and determines the value stored in the memory cell accordingly.

[5] However, the structure described above cannot be used in a parallel sense amplifier, wherein the input current must be compared with multiple reference values at the same time; a typical application of this sense amplifier is the reading in parallel mode of a non-volatile multilevel memory device. Indeed, in this case it is difficult to impossible to mirror the different reference currents (provided to respective input branches) into the same output branch connected to the memory cell.

[6] A known solution is that of using a load including a diode-connected transistor in each branch of the sense amplifier (both the input branch and the output branch). In this way, each reference current is mirrored into an input terminal of a corresponding comparator, while the current of the memory cell is mirrored into the other input terminals of all the comparators. The currents being input to each comparator generate a corresponding voltage, which allow establishing whether the current of the memory cell is lower or higher than the corresponding reference current. The combination of the results of the different comparisons identifies the value stored in the memory cell.

[7] A drawback of the structure described above is that the voltages being input to the different comparators typically have very low values (since the load transistors in the corresponding current mirrors exhibit a negligible resistance). Therefore, the sense amplifier is rather inaccurate.

[8] Moreover, the several current mirrors consume a relatively high amount of static power. These current mirrors also introduce further inaccuracies owing to the unavoidable tolerances of the manufacturing processes.

[9] A different sense amplifier (of the non-parallel type) is described in U.S. Patent 6,128,225. In this case, the current of the memory cell is provided to the input branch of the current mirror so as to be reflected to the output branch connected to the reference cell. Nevertheless, this sense amplifier can be used only in a standard memory device. Indeed, the current mirror has unbalanced loads. Therefore, the sense amplifier is incompatible with a parallel sense amplifier (particularly, for use in a multilevel memory device).

SUMMARY

[10] An embodiment of the present invention is a parallel sense amplifier that overcomes the above-mentioned drawbacks. Briefly, the parallel sense amplifier includes a measuring branch for receiving an input current to be measured, a plurality of reference branches each for receiving a corresponding reference current, and a plurality of comparators each for comparing a voltage at a measuring node along the measuring branch with a voltage at a reference node along a

corresponding reference branch; the amplifier further including a multiple current mirror for mirroring the input current into each reference branch.

[11] Moreover, a memory device comprising the sense amplifier and a corresponding method of operating the sense amplifier are also encompassed.

BRIEF DESCRIPTION OF THE DRAWINGS

[12] Further features and advantages of the present invention will be made clear by the following description of embodiments thereof, given purely by way of a non-restrictive example, with reference to the attached figures, in which:

[13] **FIG. 1** is a schematic block diagram of a memory device in which a sense amplifier according to an embodiment of the present invention can be used;

[14] **FIG. 2** shows a sense amplifier known in the art;

[15] **FIG. 3a** is a simplified circuit scheme of a sense amplifier according to an embodiment of the invention; and

[16] **FIG. 3b** illustrates functional blocks used for producing some control signals for the sense amplifier of **FIG. 3a** according to an embodiment of the invention.

DETAILED DESCRIPTION

[17] With reference in particular to **FIG. 1**, a non-volatile multilevel memory device ***100*** (for example, an asynchronous EPROM) is shown according to an embodiment of the invention. The memory device ***100*** includes a matrix of memory cells ***105***. Each memory cell consists of a floating gate MOS transistor (not shown in **FIG. 1**). The memory cell can be programmed to multiple levels, which are associated with corresponding ranges of its threshold voltage (depending on the electrical charge accumulated in the floating gate). Each level represents a different logical value; for example, the memory cell may support 4 levels, so that it stores a logical value that includes 2 bits of information B_1B_0 (11, 10 01 and 00 for increasing threshold voltages). The matrix ***105*** is partitioned into a plurality of sectors (for example, 16 sectors each one storing 4M bits). For each sector, the matrix ***105*** includes a set of reference cells, which are programmed to preset threshold voltages.

[18] A column decoder ***110c*** and a row decoder ***110r*** are used for selecting a set of memory cells of the matrix ***105*** in response to an address ADR; for example, the set may include 8 memory cells, which store a word ***WD*** of 16 bits. The address ***ADR*** is received asynchronously from outside the memory device ***100***; the address ***ADR*** is applied to a buffer ***115***, which drives the decoders ***110c*** and ***110r*** accordingly. The column decoder ***110c*** also interfaces with a reading and writing unit (R/W) ***120***; the unit ***120*** includes the circuits that are needed for reading a word ***WD*** from and for writing a word ***WD*** to the selected memory cells.

[19] The address ***ADR*** in the buffer ***115*** is also provided to an Address Transition Detection (ATD) circuit ***125***; the ATD circuit ***125*** generates a detecting pulse ***DET*** whenever the address ***ADR*** switches. The detection pulse ***DET*** is applied to a controller ***130***, which outputs a sequence of control signals (denoted as a whole with Sc) for the other units of the memory device ***100***; for example, the controller ***130*** triggers the execution of a reading operation from the matrix ***105*** in response to the detection pulse ***DET***.

[20] For this purpose, each selected memory cell is suitably biased so as to supply a current ***Im*** corresponding to the logical value that is stored. Particularly, the memory cell at the logical value ***11*** exhibits a low threshold voltage, and therefore supplies a high current ***Im***; the current ***Im*** lowers as the threshold voltage increases, until ideally it is zero when the memory cell is at the logical value ***00***. Each pair of adjacent logical values is discriminated by a reference current Ir_j (with j=0...2 in the case at issue), which is provided by a corresponding reference cell; for example, the memory cell is deemed at the level ***10*** when its current ***Im*** is between the reference current Ir_1 and the reference current Ir_2. To this end, for each selected memory cell the reading and writing unit ***120*** includes a parallel sense amplifier; as described in detail in the following, the sense amplifier simultaneously compares the cell current ***Im*** with the reference currents Ir_0-Ir_2.

[21] However, the concepts disclosed herein are also applicable when the memory device has another architecture or it is of a different type (for example, a flash E^2PROM). Similar considerations apply if the memory cells are programmable to another number of levels (also different from a power of 2), if the matrix is

partitioned into a different number of sectors, if the sectors and/or the words have different size, and the like.

[22] Considering now **FIG. 2**, a parallel sense amplifier ***200*** known in the art is shown. The sense amplifier ***200*** includes a matrix branch ***205m***, which receives the cell current ***Im*** at its input node ***207m***; three reference branches ***205r$_0$-205r$_2$*** instead receive the corresponding reference currents ***Ir$_0$-Ir$_2$*** at their respective input nodes ***207r$_0$-207r$_2$***. In the figure, a selected memory cell ***Cm*** and three reference cells ***Cr$_0$-Cr$_2$*** (which provide the reference currents ***Ir$_0$-Ir$_2$***) are shown as if they were directly connected to the matrix branch ***205m*** and to the corresponding reference branches ***205r$_0$-205r$_2$***, respectively (omitting the column decoder for the sake of simplicity). Each (memory and reference) cell ***Cm,Cr$_0$-Cr$_2$*** has the source terminal that is maintained at a reference voltage (or ground), and the drain terminal that is connected to the corresponding input node ***207m,207r$_0$-207r$_2$*** of the sense amplifier ***200***; the control gate terminals of all the cells ***Cm,Cr$_0$-Cr$_2$*** receive a reading voltage equal to a bootstrap voltage, which is higher than a power supply voltage +Vdd of the memory device (for example, 5V and 1.8V with respect to ground).

[23] Each branch ***205m,205r$_0$-205r$_2$*** includes a corresponding diode-connected PMOS transistor ***210m,210r$_0$-210r$_2$***. Particularly, the transistors ***210m,210r$_0$-210r$_2$*** have respective source terminals that are connected to a power supply terminal (which provides the voltage +Vdd), and the gate terminals that are short-circuited to their drain terminals.

[24] A pre-charging block (PC) ***215m,215r$_0$-215r$_2$*** is connected in series to each transistor ***210m,210r$_0$-210r$_2$*** (between the drain terminal of the transistor ***210m,210r$_0$-210r$_2$*** and the input terminal ***207m,207$_0$-207$_2$***). Each pre-charging block ***215m,215r$_0$-215r$_2$*** is used to bring the voltage at the drain terminal of the corresponding cell ***Cm,Cr$_0$-Cr$_2$*** towards the correct biasing value (for example, 1V) very fast. Moreover, an equalizing NMOS transistor ***220r$_0$-220r$_2$*** joins each reference branch ***205r$_0$-205r$_2$*** to the matrix branch ***205m***. Particularly, each equalizing transistor ***220r0-220r2*** has a drain terminal that is connected to the corresponding input node ***207r$_0$-207r$_2$*** and a source terminal that is connected to the input node ***207m***.

[25] The gate terminals of the equalizing transistors ***220r$_0$-220r$_2$*** are controlled by an enabling signal ***EN*** and the pre-charging blocks ***215m,215r$_0$-215r$_2$*** are controlled by the same enabling signal being negated ***$\underline{EN}$*** (the signal ***EN*** is at the logical level 0 when deasserted and at the logical level 1 when asserted; conversely, the signal ***$\underline{EN}$*** is at the logical level 1 when deasserted and at the logical level 0 when asserted). The enabling signals ***EN,$\underline{EN}$*** are asserted at the beginning of the reading operation (by the controller of the memory device in response to the detection pulse ***DET***); those signals ***EN,$\underline{EN}$*** have a length ensuring that the sense amplifier ***200*** is brought to a correct starting condition.

[26] A respective comparator ***225r$_0$-225r$_2$*** (including a differential amplifier) is associated with each reference branch ***205r$_0$-205r$_2$***. Particularly, the inverting input terminal of each comparator ***225r$_0$-225r$_2$*** is connected to the drain terminal of the corresponding transistor ***210r$_0$-210r$_2$***; the non-inverting input terminals of all the comparators ***225r$_0$-225r$_2$*** are instead connected to the drain terminal of the transistor ***210m***. In this way, each transistor ***210m,210r$_0$-210r$_2$*** forms a current mirror with a corresponding transistor within the comparator ***225r$_0$-225r$_2$*** to which it is connected. The output terminal of each comparator ***225r$_0$-225r$_2$*** generates a signal ***Rr$_0$-Rr$_1$*** indicative of the result of the comparison; those comparison signals ***Rr$_0$-Rr$_1$*** are applied to an encoder ***230***, which provides the bits ***B$_1$B$_0$*** stored in the memory cell ***Cm***.

[27] During the reading operation, the cell current ***Im*** is mirrored into the non-inverting input terminals of all the comparators ***225r$_0$-225r$_2$***; at the same time, each reference current ***Ir$_0$-Ir$_2$*** is mirrored into the inverting input terminal of the corresponding comparator ***225r$_0$-225r$_2$***. The comparators ***225r$_0$-225r$_2$*** then perform a current measure; particularly, the comparison signal ***Rr$_0$-Rr$_2$*** of each comparator ***225r$_0$-225r$_2$*** is asserted when the cell current ***Im*** is higher than the corresponding reference current ***Ir$_0$-Ir$_2$***. In this way, the combination of the comparison signals ***Rr$_0$-Rr$_2$*** univocally identifies the level of (*i.e.,* the data stored in) the memory cell ***Cm*** (with the corresponding logical value ***B$_1$B$_0$*** that is then obtained by the encoder ***230***).

[28] Referring to **FIG. 3a**, a sense amplifier ***300*** according to an embodiment of the present invention is instead shown (the elements corresponding to the ones shown in **FIG. 2** are denoted with the same references and their

explanation is omitted for the sake of brevity). In sharp contrast to the solution known in the art (**FIG. 2**), the sense amplifier ***300*** includes a multiple current mirror; this current mirror has an input branch being included in the matrix branch ***205m*** and three output branches each one being included in a corresponding reference branch ***205r$_0$-205r$_2$***.

[29] Particularly, only the matrix branch ***205m*** has a PMOS transistor ***305m*** (corresponding to the transistor ***210m*** of **FIG. 2**) that is diode-connected; the reference branches ***205r$_0$-205r$_2$*** instead include PMOS transistors ***305r$_0$-305r$_2$*** (corresponding to the transistors ***210r$_0$-210r$_2$*** of **FIG. 2**) having their gate terminals that are connected to the gate terminal of the transistor ***305m***. The transistors ***305m,305r$_0$-305r$_2$*** have substantially the same size; as a consequence, the mirror factor of the structure so obtained (between the input branch and each output branch) is equal to 1.

[30] Contrary to the preceding case, the drain terminal of the transistor ***305m*** (node ***310m***) is connected to the inverting input terminal of all the comparators ***225r$_0$-225r$_2$***, while the drain terminal of each transistor ***305r$_0$-305r$_2$*** (node ***310r$_0$-310r$_2$***) is connected to the non-inverting input terminal of the corresponding comparator ***225r$_0$-225r$_2$***.

[31] Moreover, the gate terminals of the equalizing transistors ***220r$_0$-220r$_2$*** are now controlled by an enabling signal ***EQ***, while the pre-charging blocks ***215m,215r$_0$-215r$_2$*** are controlled by a different (negated) enabling signal ***EQd*** (which signals are generated by the controller of the memory device, as described in detail below).

[32] During the reading operation, the cell current ***Im*** (in the matrix branch ***205m***) is mirrored into all the reference branches ***205r$_0$-205r$_2$***.

[33] For each reference branch ***205r$_j$***, let us consider the case in which the cell current ***Im*** is higher than the reference current ***Ir$_j$***. During a transient phase, the difference between the cell current ***Im*** and the reference current ***Ir$_j$*** loads a stray capacitor associated with the node ***310r$_j$***; the voltage at this node ***310r$_j$*** then raises towards the power supply voltage +Vdd, updating the biasing condition of the transistor ***305r$_j$***. In a steady state, the transistor ***305r$_j$*** will then work in the resistive

zone conducting the current Ir_j supplied by the reference cell Cr_j (with the structure $305m,305r_j$ that does not operate as a current mirror any longer). As a consequence, the voltage at the non-inverting input terminal of the corresponding comparator $225r_j$ is higher than the voltage at its inverting input terminal, so that the comparison signal Rr_j is asserted.

[34] The opposite situation arises when the cell current ***Im*** is lower than the reference current Ir_j. During a transient phase, the difference between the reference current Ir_j and the cell current ***Im*** discharges the stray capacitor associated with the node $310r_j$; the voltage at this node $310r_j$ then lowers towards ground, updating the biasing condition of the reference cell Cr_j. In a steady state, the reference cell Cr_j will then supply the cell current ***Im*** forced by the current mirror $305m,305r_j$. As a consequence, the voltage at the non-inverting input terminal of the corresponding comparator $225r_j$ is lower than the voltage at its inverting input terminal, so that the comparison signal Rr_j is deasserted.

[35] In this way, the above-described structure implements a current-to-voltage conversion with a gain on an input stage of the sense amplifier ***300***. The comparators $225r_0$-$225r_2$ then perform a voltage measure on values that are relatively high. This ensures a good sensitivity of the sense amplifier ***300*** (even with power supply voltages of low value).

[36] Such a characteristic may be particularly important during a writing operation on the memory device. Typically, the writing of a word is obtained through a series of programming steps, each one followed by a verification of the values actually stored in the selected memory cells. The verification is performed reading the written word with a safety margin, wherein the cell current ***Im*** is compared with reference currents corresponding (for each logical value) to narrower ranges of the distribution of its threshold voltage. In this case, it is then necessary to discriminate current differences of very low value.

[37] Moreover, it should be noted that in the above-described structure only the gate terminal of the transistor ***305m*** is connected as an input to the comparators $225r_0$-$225r_2$. Therefore, owing to the capacitive coupling between this gate terminal and the power supply terminal (due to a corresponding stray capacitor), any noise on the power supply voltage +Vdd is reflected identically into the voltage at the inverting

input terminals of all the comparators ***225r$_0$-225r$_2$***. Conversely, the gate terminals of the transistors ***305r$_0$-305r$_2$*** are not connected as an input to the comparators ***225r$_0$-2255r$_2$*** any longer; therefore, the voltage at the non-inverting input terminals of the respective comparators ***225r$_0$-225r$_2$*** is less affected, or not affected at all, by any noise on the power supply voltage +Vdd.

[38] As shown in **FIG. 3b**, the controller of the memory device generates the enabling signals ***EQ*** and ***EQd*** in response to the detection pulse ***DET*** according to an embodiment of the invention. Particularly, the detection pulse ***DET*** is provided to a delay generator ***350***, which outputs the enabling signal ***EQ***; the enabling signal ***EQ*** consists of a square wave that is triggered by the detection pulse ***DET*** and has a preset length (for example, some ns).

[39] In turn, the enabling signal ***EQ*** is provided to a further delay generator ***355***, which outputs a signal ***EQd***; the signal ***EQd*** switches in response to the enabling signal ***EQ***, and maintains this state for a time that is longer (for example, of some ns) than the length of the enabling signal ***EQ***. The negated enabling signal ***EQd*** is then obtained from the signal ***EQd*** through an inverter ***360***.

[40] However, the concepts discussed herein are also applicable when the PMOS transistors are replaced with NMOS transistors, and vice-versa, or when the sense amplifier includes equivalent components. Similar considerations apply if equalization blocks with a different structure are provided, if the enabling signals are in phase, and the like.

[41] More generally, a parallel sense amplifier according to an embodiment of the invention includes a measuring branch for receiving an input current to be measured, and a plurality of reference branches each one for receiving a reference current. Moreover, a plurality of comparators are provided, each one for comparing a voltage at a measuring node along the measuring branch with a voltage at a reference node along a corresponding reference branch. The amplifier further includes a multiple current mirror for mirroring the input current into each reference branch.

[42] Such a parallel sense amplifier typically ensures a high accuracy (thanks to the current-to-voltage conversion with a gain on the input stage, which allows the comparators to perform a voltage measure on relatively high values).

[43] The reduction of the mirror branches significantly cuts down the power consumption in a static condition. This also avoids any inaccuracies due to the tolerances of the manufacturing processes.

[44] Moreover, such a parallel sense amplifier is typically substantially insensitive to the noise on the power supply voltage.

[45] The embodiments of the invention described above offer further advantages.

[46] Particularly, the current mirror has a mirroring factor equal to 1.

[47] This sense amplifier is specifically designed for use in a non-volatile multilevel memory device.

[48] A suggested choice for the implementation of the current mirror envisages a single diode-connected transistor (in the input branch).

[49] The proposed structure is particularly simple and compact.

[50] The different transistors have substantially the same size.

[51] However, alternative embodiments of the sense amplifier are contemplated; moreover, different sizes of the transistors that form the current mirror (and then a different mirroring factor) are not excluded.

[52] As a further enhancement, the pre-charging blocks and the equalizing blocks may be controlled by enabling signals having a different length.

[53] The longer length of the pre-charging phase typically improves the operation of the sense amplifier.

[54] The enabling signals may be generated using suitable delay generators.

[55] The proposed solution is very simple, but at the same time effective.

[56] However, the sense amplifier according to the above-described embodiment of the present invention lends itself to be implemented generating the

enabling signals in a different way, or even with a single enabling signal for both the pre-charging blocks and the equalizing blocks.

[57] The proposed embodiments of the sense amplifier are specifically designed for use in a non-volatile multilevel memory device, although they may be used in other types of memory devices.

[58] Advantageously, the memory device may be of the asynchronous type (in which case, the different enabling signals cited above are generated from an address transition detection signal).

[59] However, different applications of the embodiments of the sense amplifier are not excluded; for example, the sense amplifier can be used in a synchronous memory device, or even in apparatuses of different type (for example, in a sensor).

[60] Furthermore, an electronic system such as a computer system may incorporate a memory device that includes the parallel sense amplifier ***300*** (or other embodiment of the parallel sense amplifier) according to an embodiment of the invention.

[61] Naturally, in order to satisfy local and specific requirements, a person skilled in the art may apply to the embodiments described above many modifications and alterations all of which, however, are included within the spirit and scope of the invention.